SYNOPSYS INC
Form 10-K
December 15, 2014
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UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 10-K

(Mark One)
ý ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934
For the year ended October 31, 2014
OR
¨ TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934
For the transition period from to
Commission File Number 0-19807

SYNOPSYS, INC.
(Exact name of registrant as specified in its charter)

Delaware	56-1546236
(State or other jurisdiction of incorporation or organization)	(I.R.S. Employer Identification No.)

700 East Middlefield Road, Mountain View, California 94043
(Address of principal executive offices, including zip code)
(650) 584-5000
(Registrant's telephone number, including area code)

Securities Registered Pursuant to Section 12(b) of the Act:

Title of Each Class	Name of Each Exchange on Which Registered
Common Stock, $0.01 par value	NASDAQ Global Select Market

Securities Registered Pursuant to Section 12(g) of the Act: None
Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes ý No ¨
Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes ¨ No ý

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes ý No ¨
Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Web site, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T (§ 232.405 of this chapter) during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files). Yes ý No ¨

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K (§ 229.405 of this chapter) is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. ý

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting company. See definitions of "large accelerated filer," "accelerated filer" and "smaller reporting company" in Rule 12b-2 of the Exchange Act. (Check one):

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Large accelerated filer x Accelerated filer ¨ Non-accelerated filer ¨ Smaller Reporting Company ¨
(Do not check if a smaller reporting company)

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Exchange Act). Yes ¨ No ý

The aggregate market value of the voting and non-voting common equity held by non-affiliates computed by reference to the price at which the common equity was last sold as of the last business day of the registrant's most recently completed second fiscal quarter was approximately $3.8 billion. Aggregate market value excludes an aggregate of approximately 53.9 million shares of common stock held by the registrant's executive officers and directors and by each person known by the registrant to own 5% or more of the outstanding common stock on such date. Exclusion of shares held by any of these persons should not be construed to indicate that such person possesses the power, direct or indirect, to direct or cause the direction of the management or policies of the registrant, or that such person is controlled by or under common control with the registrant.

On December 10, 2014, 153,103,327 shares of the registrant's Common Stock, $0.01 par value, were outstanding.

DOCUMENTS INCORPORATED BY REFERENCE

Portions of the registrant's Proxy Statement relating to the registrant's 2015 Annual Meeting of Stockholders, scheduled to be held on April 2, 2015, are incorporated by reference into Part III of this Annual Report on Form 10-K where indicated. Except as expressly incorporated by reference, the registrant's Proxy Statement shall not be deemed to be part of this report.

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ANNUAL REPORT ON FORM 10-K
Year ended October 31, 2014
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Cautionary Note Regarding Forward-Looking Statements

This Annual Report on Form 10-K (this Form 10-K or Annual Report) contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933, as amended (the Securities Act) and Section 21E of the Securities Exchange Act of 1934, as amended (the Exchange Act), which are subject to the "safe harbor" created by those sections. Any statements herein that are not statements of historical fact may be deemed to be forward-looking statements. For example, words such as "may," "will," "could," "would," "should," "anticipate," "expect," "intend," "believe," "project" or "continue" and the negatives of such terms are intended to identify forward-looking statements. This Form 10-K includes, among others, forward-looking statements regarding our expectations about:

- our business, product and platform strategies;
- our business outlook;
- prior and future acquisitions, including the expected benefits of completed acquisitions;
- the impact of macroeconomic conditions on our business and our customers' businesses;
- demand for our products and our customers' products;
- customer license renewals;
- the completion of development of our unfinished products, or further development, integration, or broader release of our existing products;
- technological trends in integrated circuit design;
- our ability to successfully compete in the electronic design automation industry;
- the continuation of current industry trends towards vendor and customer consolidation;
- our license mix;
- litigation;
- our ability to protect our intellectual property rights;
- our cash, cash equivalents and cash generated from operations; and
- our future liquidity requirements.

These statements involve certain known and unknown risks, uncertainties and other factors that could cause our actual results, time frames or achievements to differ materially from those expressed or implied in our forward-looking statements. Accordingly, we caution readers not to place undue reliance on these statements. Such risks and uncertainties include, among others, those listed in Part I, Item 1A, Risk Factors of this Form 10-K. The information included herein represents our estimates and assumptions as of the date of this filing. Unless required by law, we undertake no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future. All subsequent written or oral forward-looking statements attributable to Synopsys or persons acting on our behalf are expressly qualified in their entirety by these cautionary statements. Readers are urged to carefully review and consider the various disclosures made in this report and in other documents we file from time to time with the Securities and Exchange Commission (SEC) that attempt to advise interested parties of the risks and factors that may affect our business.

Fiscal Year End

Our fiscal year generally ends on the Saturday nearest to October 31 and consists of 52 weeks, with the exception that approximately every five years, we have a 53-week year.

Fiscal 2014 and 2013 were 52-week years ending on November 1, 2014 and November 2, 2013, respectively. Fiscal 2012 was a 53-week year ending on November 3, 2012. The extra week in fiscal 2012 resulted in approximately $26 million of additional revenue, related primarily to time-based licenses, and approximately $16 million of additional expenses.

For presentation purposes, this Form 10-K refers to October 31 as the end of our fiscal year.

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PART I

Item 1. Business

Introduction

Synopsys, Inc. is a global leader in providing software, intellectual property and services used to design integrated circuits and electronic systems. For more than 25 years, we have supplied the electronic design automation (EDA) software that engineers use to design and test integrated circuits (ICs), commonly called chips. We also provide intellectual property (IP) products, which are pre-designed circuits that engineers use as components of larger chip designs instead of designing those circuits themselves. We provide software and hardware used to develop the electronic systems that incorporate chips and the software that runs on them. To complement these product offerings, we provide technical services to support our solutions and help our customers develop chips and electronic systems. We are also a leading provider of software tools that developers use to improve the quality, security, and time-to-market of software code in a wide variety of industries, including electronics, financial services, energy, and industrials.

Corporate Information

We incorporated in 1986 in North Carolina and reincorporated in Delaware in 1987. Our headquarters are located at 700 East Middlefield Road, Mountain View, California 94043, and our telephone number there is (650) 584-5000. We expect that our headquarters will change to 690 East Middlefield Road, Mountain View, California 94043, in early 2015. We have approximately 98 offices worldwide.

Our annual and quarterly reports on Forms 10-K and 10-Q (including related filings in XBRL format), current reports on Form 8-K, and Proxy Statements relating to our annual meetings of stockholders, including any amendments to these reports, as well as filings made by our executive officers and directors, are available through the Investor Relations page of our Internet website (www.synopsys.com) free of charge as soon as practicable after we file them with, or furnish them to, the SEC (www.sec.gov). We use our Investor Relations page as a routine channel for distribution of important information, including news releases, analyst presentations, and financial information. The contents of our website are not part of this Form 10-K.

Background

Recent years have seen a remarkable proliferation of consumer and wireless electronic products, particularly mobile devices. The growth of the Internet and cloud computing has provided people with new ways to create, store and share information. At the same time, the increasing use of electronics in cars, buildings, and appliances and other consumer products is expanding the landscape of “smart” devices.

These developments depend, in large part, on chips. It is common for a single chip to combine many components (processor, communications, memory, custom logic, input/output) into a single System-on-Chip (SoC), resulting in highly complex chip designs. The most complex chips today contain more than a billion transistors, the basic building blocks for integrated circuits, each of which may have features that are less than 1/1,000th the diameter of a human hair. At such small dimensions, the wavelength of light itself can become an obstacle to production, becoming too big to create such dense features and requiring creative and complicated new approaches from designers. Designers have turned to new manufacturing techniques, such as double patterning lithography and FinFET transistors, which introduce their own challenges in design and production.

In addition, due to the popularity of mobile devices and other electronic products, there is increasing demand for integrated circuits and systems with greater functionality and performance, reduced size, and less power consumption. The designers of these products—our customers—are facing intense pressure to deliver innovative products at ever shorter times-to-market, as well as at lower prices. In other words, innovation in chip and system design often hinges on “better,” “sooner,” and “cheaper.”

A similar dynamic is at work in the software industry, where the pace of innovation requires developers to deliver high quality software, which can include millions of lines of code, in increasingly shrinking release cycles. Bugs, defects, and security vulnerabilities in code can be difficult to detect and expensive to fix. But, at a time when software is prevalent in many industries and in an increasing array of smart devices, it can be crucial to do so.

Synopsys is at the heart of accelerating innovation in the electronics industry. We provide the software tools, IP, hardware and other technologies that designers use to create chips and systems. We also provide the software tools that software developers use to detect critical flaws in their code.

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The task of the chip and system designer is to determine how best to locate and connect the building blocks of chips, verifying that the resulting design behaves as intended and ensuring that the design can be manufactured efficiently and cost-effectively. This task is a complicated, multi-step process that is both expensive and time-consuming. We offer a wide range of products that help designers at different steps in the overall design process, both for the design of individual integrated circuits and for the design of larger systems. Our products can increase designer productivity and efficiency by automating tasks, keeping track of large amounts of design data, adding intelligence to the design process, facilitating reuse of past designs and reducing errors. Our IP products offer proven, high-quality pre-configured circuits that are ready-to-use in a chip design, saving customers time and enabling them direct resources to features that differentiate their products. Our global service and support engineers also provide expert technical support and design assistance to our customers.

The task of the software developer is to write code that not only accomplishes the developer's goal as efficiently as possible but that also runs securely and free of errors. We offer products that can help developers write better, more secure code by analyzing their code for quality defects and security vulnerabilities, adding intelligence and automation to the software testing process, and helping to eliminate quality and security defects in a systematic manner. Our products can enable software developers to catch flaws earlier in the development cycle, when they can be less costly to fix.

Products and Services

Revenue from our products and services is reported in four groups:

- Core EDA, which includes our digital and custom IC design products, our verification products, and our field-programmable gate array (FPGA) design products;
- IP and Software Solutions, which includes our DesignWare® IP portfolio, our system-level design tools, and our Coverity® software quality and security testing solutions;
- Manufacturing Solutions; and
- Professional Services.

Core EDA Solutions

The process of designing integrated circuits contains many complex steps: architecture definition, RTL (register transfer level) design, functional/RTL verification, logic design or synthesis, gate-level verification, floorplanning, and place and route, to name just a few. Designers use our Core EDA products to automate the integrated circuit design process and to reduce errors. We offer a large number of Core EDA products intended to address the process comprehensively. Our Core EDA products generally fall into the following categories:

- Digital and Custom IC Design, which includes tools to design an integrated circuit;
- Verification, which includes technology to verify that an integrated circuit behaves as intended; and
- FPGA Design, which includes tools to design FPGAs, a complex, configurable form of integrated circuit.

Digital and Custom IC Design

Our Galaxy™ Design Platform provides our customers with a single, integrated chip design solution that includes industry-leading individual products and incorporates common libraries and consistent timing, delay calculation and constraints throughout the design process. The platform allows designers the flexibility to integrate internally developed and third-party tools. With this advanced functionality, common foundation and flexibility, our Galaxy Design Platform helps reduce design times, decrease integration costs and minimize the risks inherent in advanced, complex integrated circuit designs. Our products span digital, custom and analog/mixed-signal designs.

In fiscal 2014, we introduced our IC Compiler™ II physical design solution and expect to continue to broaden its availability in fiscal 2015. IC Compiler II is a complete place-and-route system, built on new, multi-threaded infrastructure, that offers faster runtime, uses less memory, and delivers superior chip design results in area, timing, and power, which can help designers reduce their design iterations and boost design productivity.

Our other principal design products, also available as part of the Galaxy Design Platform, are our IC Compiler physical design solution, Design Compiler® logic synthesis product, Galaxy Custom Designer® and Laker® Layout

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custom design solutions, CustomSim™ tool for analog/mixed-signal verification, PrimeTime® timing analysis products, StarRC™ product for extraction, and IC Validator tool for physical verification.

Verification

In fiscal 2014, we introduced our Verification Continuum™ Platform to accelerate industry innovation by enabling earlier software bring-up and shorter times-to-market for advanced SoCs. Verification Continuum is built from our industry-leading and fastest verification technologies, providing virtual prototyping, static and formal verification, simulation, emulation, FPGA-based prototyping, and debug in a unified environment with verification IP and planning and coverage technology. Elements of the platform are in various stages of release, with some elements available currently and others expected to be generally available in calendar year 2015.

The individual products included in Verification Continuum span both our Core EDA and IP and Software Solutions revenue groups. The solutions reported in Core EDA revenue include the following:

- Our Verification Compiler™ solution, released in fiscal 2014, which is a complete portfolio of integrated, next-generation verification technologies that include advanced debug (our Verdi® solution), simulation (our VCS® comprehensive RTL verification technology), new static and formal verification technology, verification IP, and planning and coverage technology. In addition to their inclusion in our Verification Compiler solution, these verification technologies also continue to be sold as individual point tools.
- ZeBu® emulation systems, which use high-performance hardware to emulate SoC designs so that designers can accelerate verification of large complex SoCs and perform earlier verification of the SoC together with software.
- Our other principal individual verification solutions, including CustomSim™ FastSPICE and FineSim® SPICE/FastSPICE circuit simulation and analysis products, HSPICE® circuit simulator, and CustomExplorer™ Ultra mixed-signal regression and analysis environment.

The virtual prototyping and FPGA-based prototyping solutions that are part of our Verification Continuum platform are included in our IP and Software Solutions revenue group.

FPGA Design

FPGAs are complex chips that can be customized or programmed to perform a specific function after they are manufactured. For FPGA design, we offer Synplify® Pro and Premier implementation and Identify® debug software tools.

IP and Software Solutions

IP Products

As more functionality converges into a single device or even a single chip, and chip designs grow more complex, the number of third-party IP blocks incorporated into designs is rapidly increasing. Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoCs. Our broad DesignWare® IP portfolio includes:

- high-quality solutions for widely used interfaces such as USB, PCI Express, DDR, Ethernet, SATA, MIPI, and HDMI;
- analog IP for analog-to-digital data conversion and audio;
- SoC infrastructure IP including minPower datapath components, ARM® AMBA® interconnect fabric and peripherals, and verification IP;
- logic libraries and embedded memories, including SRAMs and non-volatile memory;
- configurable processor cores and application-specific instruction-set processors (ASIPs) for embedded and deeply embedded designs; and
- IP subsystems for audio and sensor functionality that combine IP blocks and software into an integrated, pre-verified solution.

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Our IP Accelerated initiative augments our established, broad portfolio of silicon-proven DesignWare IP with DesignWare IP Prototyping Kits, DesignWare IP Virtual Development Kits, and customized IP subsystems to accelerate prototyping, software development, and integration of IP into SoCs.

System-Level Solutions

Optimizing the system-level design earlier in the development cycle, including both hardware and software components, is increasingly important for customers to meet their performance, time-to-market, and development cost goals. Synopsys has the industry's broadest portfolio of tools, models and services for the system-level design of SoCs. Our Platform Architect™ software enables early and rapid exploration of SoC architectural trade-offs. To speed the creation, implementation and verification of differentiated IP blocks, we offer SPW™ and System Studio™ tools for algorithm design, Processor Designer™ software for custom processor design, and Synphony Model™ and C Compilers for high-level synthesis.

Escalating software content and complexity in today's electronic devices are driving the adoption of new tools and methods to accelerate software development and ease hardware-software integration and system validation. Our system-level portfolio includes prototyping technologies that can improve the productivity of both hardware and software development teams. These prototyping technologies are also an important component of our Verification Continuum Platform. Our Virtualizer™ tool and broad portfolio of transaction-level models enable the creation of virtual prototypes, fully functional software models of complete systems that enable engineers to start software development up to twelve months earlier than traditional methods. Our HAPS® FPGA-based prototyping systems integrate high performance hardware and software tools with real-world interfaces to enable faster hardware-software integration and full system validation. Our hybrid prototyping solution combines both approaches to prototyping, integrating Virtualizer virtual prototyping with HAPS FPGA-based prototyping.

Synopsys also provides a series of tools used in the design of optical systems and photonic devices. Our CODE V® solution enables engineers to model, analyze and optimize designs for optical imaging and communication systems. Our LightTools® design and analysis software allows designers to simulate and improve the performance of a broad range of illumination systems, from vehicle lighting to projector systems.

Software Solutions

In the second quarter of fiscal 2014, we acquired Coverity, Inc. (Coverity), a leading provider of software quality, testing, and security tools. Coverity products help software developers reduce the risk of errors and security defects in their code before it is released. Our Coverity Code Advisor solution includes the Quality Advisor™ and Security Advisor™ tools, which analyze software code to find crash-causing bugs, incorrect program behavior, memory leaks and other flaws that degrade performance, security vulnerabilities, violations of security best practices, and other critical code issues, many of which may be difficult to detect by other means. Our Coverity Test Advisor™ solutions allow developers to focus their test development on the most critical code and to prioritize their test execution for the tests that are the most relevant for a particular set of code additions or changes. Our Coverity Connect™ platform assists software development teams in tracking and managing their code issues.

Manufacturing Solutions

Our Manufacturing Solutions products and technologies enable semiconductor manufacturers to more quickly develop new fabrication processes that produce production-level yields. These products are used in the early research and development phase and the production phase. In the production phase, manufacturers use these products to convert IC design layouts into the masks used to manufacture the devices.

Our Manufacturing Solutions include Sentaurus™ Technology-CAD (TCAD) device and process simulation products, Proteus optical proximity correction (OPC) and lithography rule check (LRC) products, CATS® mask data preparation product, and Yield Explorer® and Odyssey/Yield Manager Yield Management solutions.

Professional Services and Training

Synopsys provides consulting and design services that address all phases of the SoC development process. These services assist our customers with new tool and methodology adoption, chip architecture and specification development, functional and low-power design and verification, and physical implementation and signoff. We also provide a broad range of expert training and workshops on our latest tools and methodologies.

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Customer Service and Technical Support

A high level of customer service and support is critical to the adoption and successful use of our products. We provide technical support for our products through both field-based and corporate-based application engineering teams. Customers who purchase Technology Subscription Licenses (TSLs) receive software maintenance services bundled with their license fee. Customers who purchase term licenses and perpetual licenses may purchase these services separately. See Product Sales and Licensing Agreements below.

Software maintenance services include minor product enhancements, bug fixes and access to our technical support center for primary support. Software maintenance also includes access to the SolvNet® portal, our web-based support solution that gives customers access to Synopsys' complete design knowledge database. Updated daily, the SolvNet portal includes documentation, design tips and answers to user questions. Customers can also engage, for additional charges, our worldwide network of applications consultants for additional support needs.

In addition, Synopsys also offers training workshops designed to increase customer design proficiency and productivity with our products. Workshops cover our products and methodologies used in our design and verification flows, as well as specialized modules addressing system design, logic design, physical design, simulation and test. We offer regularly scheduled public and private courses in a variety of locations worldwide, as well as Virtual Classroom on-demand and live online training.

Product Warranties

We generally warrant our products to be free from defects in media and to substantially conform to material specifications for a period of 90 days for our software products and for up to 6 months for our HAPS FPGA-based prototyping systems. In many cases, we also provide our customers with limited indemnification with respect to claims that their use of our software products infringes on United States patents, copyrights, trademarks or trade secrets. We have not experienced material warranty or indemnity claims to date.

Support for Industry Standards

We actively create and support standards that help our customers increase productivity, facilitate efficient design flows, improve interoperability of tools from different vendors, and ensure connectivity, functionality and interoperability of IP building blocks. Standards in the electronic design industry can be established by formal accredited organizations, industry consortia, company licensing made available to all, de facto usage, or through open source licensing.

Synopsys' products support more than 35 standards, including the most commonly used hardware description languages: SystemVerilog, Verilog, VHDL, and SystemC. Our products utilize numerous industry standard data formats, application programming interfaces, and databases for the exchange of design data among our tools, other EDA vendors' products, and applications that customers develop internally. We also comply with a wide range of industry standards within our IP product family to ensure usability and interconnectivity.

Sales, Distribution and Backlog

Our EDA and IP customers are primarily semiconductor and electronics systems companies. The customers for our Coverity software solutions products include many of these companies as well as companies in a wider array of industries, including financial services, energy, and industrials. We market our products and services principally through direct sales in the United States and principal foreign markets. We typically distribute our software products and documentation to customers electronically, but provide physical media (e.g., DVD-ROMs) when requested by the customer.

We maintain sales/support centers throughout the United States. Outside the United States, we maintain sales, support or service offices in Canada, multiple countries in Europe, Israel, Japan, China, Korea, Taiwan and other countries in Asia. Our foreign headquarters for financial and tax purposes are located in Dublin, Ireland. Our offices are further described under Part I, Item 2, Properties.

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In fiscal 2014, 2013 and 2012, an aggregate of 50%, 52% and 52%, respectively, of Synopsys' total revenue was derived from sales outside of the United States. Geographic revenue, which is based on customer server site location, is shown below as a percentage of total revenue for the last three fiscal years:

Additional information relating to domestic and foreign operations, including revenue and long-lived assets by geographic area, is contained in Note 13 of Notes to Consolidated Financial Statements in Part II, Item 8, Financial Statements and Supplementary Data. Risks related to our foreign operations are described in Part I, Item 1A, Risk Factors.

Our backlog was approximately $3.5 billion on October 31, 2014, representing a 13% increase from backlog of $3.1 billion on October 31, 2013, which resulted primarily from the renewal in fiscal 2014 of large multi-year contracts, business growth, and to a lesser extent, acquisitions. Backlog represents committed orders that are expected to be recognized as revenue over the following three years. We currently expect that $1.7 billion of our backlog will be recognized after fiscal 2015. Backlog may not be a reliable predictor of our future sales as business conditions may change and technologies may evolve, and customers may seek to renegotiate their arrangements or may default on their payment obligations. For this and other reasons, we may not be able to recognize expected revenue from backlog when anticipated.

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Revenue attributable to each of our four platforms established for management reporting purposes is shown below as a percentage of total revenue for the last three fiscal years:

*Our IP and Software Solutions platform was referred to as IP and System-Level Solutions in fiscal 2013 and 2012.

Revenue derived from Intel Corporation and its subsidiaries in the aggregate accounted for 10.5%, 11.3% and 10.5% of our total revenue in fiscal 2014, 2013 and